WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array which has memory cells arranged in a matrix, each memory cell having a first MOS transistor with a stacked gate including a first semiconductor layer and a second semiconductor layer formed on the first semiconductor layer with an inter-gate insulating film interposed therebetween;

bit lines each of which connects one end of the current path of each of the first MOS transistors in the same column in common electrically;

first word lines each of which connects the second semiconductor layers of the first MOS transistors in the same row in common;

a column selector which selects any one of the bit lines;

a column decoder which controls the column selector; and

a first row decoder which selects any one of the first word lines, at least one of the column decoder and the first row decoder including a level shift circuit which includes:

a second and a third MOS transistor each of which has one end of its current path connected electrically to a power supply potential;

a fourth MOS transistor which has a gate receiving an input signal related to an address signal,

one end of its current path connected to the other end of the current path of the second MOS transistor and to the gate of the third MOS transistor, and the other end of its current path connected electrically to the ground potential;

a fifth MOS transistor which has a gate receiving the inverted signal of the input signal, one end of its current path connected to the other end of the current path of the third MOS transistor, to the gate of the second MOS transistor and to the bit line or the first word line electrically, and the other end of its current path connected electrically to the ground potential; and

a first switch element which controls the supply of the power supply potential to the second and third MOS transistors in response to the input signal.

2. The semiconductor memory device according to claim 1, wherein the first switch element includes:

a sixth MOS transistor which has one end of its current path connected to the power supply potential, the other end of its current path connected to the one end of the current path of the second MOS transistor, and a gate receiving the input signal; and

a seventh MOS transistor which has one end of its current path connected to the power supply potential, the other end of its current path connected to the one end of the current path of the third MOS transistor,

and a gate receiving the inverted signal of the input signal.

3. The semiconductor memory device according to claim 1, wherein the level shift circuit further includes:

a first capacitor element which has one electrode input the input signal; and

a second capacitor element which has one electrode input the inverted signal of the input signal, and

the first switch element controls the supply of the power supply potential to the second and third MOS transistors according to the potential at the other electrodes of the first and second capacitor elements.

4. The semiconductor memory device according to claim 3, wherein the first switch element includes:

a sixth MOS transistor which has one end of its current path connected to the power supply potential, the other end of its current path connected to the one end of the current path of the second MOS transistor, and a gate connected to the other electrode of the first capacitor element; and

a seventh MOS transistor which has one end of its current path connected to the power supply potential, the other end of its current path connected to the one end of the current path of the third MOS transistor, and a gate connected to the other electrode of the second capacitor element.

5. The semiconductor memory device according to claim 1, wherein the level shift circuit further includes:

a second switch element which connects the other ends of the current paths of the fourth and fifth MOS transistors to the ground potential, when an enable signal to bring the level shift circuit into the operating state is asserted; and

a third switch element which connects the one end of the current path of the fourth MOS transistor to the ground potential, when the enable signal is negated.

6. The semiconductor memory device according to claim 1, wherein the first switch element breaks a connection between the second MOS transistor and the power supply potential and makes a connection between the third MOS transistor and the power supply potential, when the input signal brings the fourth and fifth MOS transistors into the on state and the off state, respectively.

7. The semiconductor memory device according to claim 1, wherein

at least one of the column decoder and the first row decoder further includes a decoder circuit which decodes the address signal to obtain an address decode signal of a first voltage level,

the input signal input to the level shift circuit is the address decode signal, and

the level shift circuit converts the address decode signal into a second voltage level different from the first voltage level.

8. The semiconductor memory device according to claim 1, wherein

the input signal input to the level shift circuit is the address signal of a first voltage level,

the level shift circuit converts the address signal into a second voltage level different from the first voltage level, and

at least one of the column decoder and the first row decoder further includes a decoder circuit which decodes the address signal converted into the second voltage level to obtain an address decode signal.

9. The semiconductor memory device according to claim 1, wherein

each of the memory cells further includes an eighth MOS transistor which has a stacked gate including a third semiconductor layer and a fourth semiconductor layer formed on the third semiconductor layer with the inter-gate insulating film interposed therebetween and one end of its current path connected to the one end of the current path of the first MOS transistor,

the semiconductor memory device further comprises:

a source line which connects the other ends of the current paths of the first MOS transistors in

common;

second word lines each of which connects the fourth semiconductor layers of the eighth MOS transistors of the memory cells in the same row in common; and

a second row decoder which selects any one of the second word lines,

the bit lines are connected to the other ends of the current paths of the corresponding eighth MOS transistors, and

the first and second semiconductor layers of each of the first MOS transistors are connected to each other electrically.

10. The semiconductor memory device according to claim 1, wherein

each of the memory cells further includes:

an eighth MOS transistor which has a stacked gate including a third semiconductor layer and a fourth semiconductor layer formed on the third semiconductor layer with the inter-gate insulating film interposed therebetween and one end of its current path connected to the one end of the current path of the first MOS transistor; and

a ninth MOS transistor which has a stacked gate including a fifth semiconductor layer and a sixth semiconductor layer formed on the fifth semiconductor layer with the inter-gate insulating film interposed

therebetween and one end of its current path connected to the other end of the current path of the eighth MOS transistor,

the semiconductor memory device further comprises:

a source line which connects the other ends of the current paths of the first MOS transistors in common;

second word lines each of which connects the fourth semiconductor layers of the eighth MOS transistors of the memory cells in the same row in common;

third word lines each of which connects the sixth semiconductor layers of the ninth MOS transistors of the memory cells in the same row in common; and

a second row decoder which selects any one of the second word lines,

the first row decoder further selects any one of the third word lines,

the bit lines are connected to the other ends of the current paths of the corresponding ninth MOS transistors,

the first and second semiconductor layers of each of the first MOS transistors are connected to each other electrically, and

the fifth and sixth semiconductor layers of each of the ninth MOS transistors are connected to each other electrically.

11. The semiconductor memory device according to claim 1, wherein

each of the memory cells further includes:

an eighth MOS transistor which has a stacked gate including a third semiconductor layer and a fourth semiconductor layer formed on the third semiconductor layer with the inter-gate insulating film interposed therebetween; and

a plurality of ninth MOS transistors which are connected in series between one end of the current path of the first MOS transistor and one end of the current path of the eighth MOS transistor and each of which has a stacked gate including a fifth semiconductor layer and a sixth semiconductor layer formed on the fifth semiconductor layer with the inter-gate insulating film interposed therebetween,

the semiconductor memory device further comprises:

a source line which connects the other ends of the current paths of the first MOS transistors in common;

second word lines each of which connects the fourth semiconductor layers of the eighth MOS transistors in the same row in common;

third word lines each of which connects the sixth semiconductor layers of the ninth MOS transistors in the same row in common; and

a second row decoder which selects any one of

the third word lines,

the first row decoder further selects any one of the third word lines,

the bit lines are connected to the other ends of the current paths of the corresponding eighth MOS transistors,

the first and second semiconductor layers of each of the first MOS transistors are connected to each other electrically, and

the third and fourth semiconductor layers of each of the eighth MOS transistors are connected to each other electrically.